DIELECTRIC ANTI-REFLECTIVE COATING SURFACE TREATMENT TO PREVENT DEFECT GENERATION IN ASSOCIATED WET CLEAN

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FIELD OF THE INVENTION

[0001] The present invention relates to the prevention of defects during a semiconductor process. More specifically, the present invention relates to a method for preventing watermark defects when an anti-reflective coating (ARC) is used in conjunction with a wet clean.

RELATED ART

[0002] Plasma-deposited silicon oxynitride ($Si_XO_YN_ZH_A$), is a dielectric material that has been used as an anti-reflective coating (ARC) on critical layers in photolithographic processes. One problem encountered with the use of silicon oxynitride is that this material is not compatible with hydrogen fluoride (HF) or buffered oxide etch (BOE) based wet clean processes. Plasma-based silicon oxynitride is a complex material having an unusually rich hydrogen (H) content of about 15% and poor film density. Moreover, the surface of plasma-based silicon oxynitride is very hydrophilic. These characteristics result in the formation of small amounts of water containing micro bumps (i.e., watermarks) on a silicon oxynitride layer when the silicon oxynitride is present during an HF or BOE based wet clean process. Some droplets may drop from the surface of the silicon

oxynitride layer onto other layers exposed by the HF or BOE wet clean process. These watermarks are difficult to remove.

[0003] The presence of watermarks can result in defects that are hereinafter referred to as watermark defects. A watermark defect is typically created when a layer is deposited over a watermark. A watermark defect can appear either immediately after the layer is deposited, or at some subsequent time.

[0004] Fig. 1 is a cross-sectional diagram of a semiconductor structure 10 including a substrate 11, pad oxide 12, shallow trench isolation (STI) material 13, and two watermark defects 14-15 located between silicon substrate 11 and STI material 13. Although Fig. 1 illustrates an STI structure, it is understood that watermark defects may exist on many other structures, and that the STI structure is simply illustrated as an example. In general, watermark defects are silicate (SiO_x), which is similar to silicon oxide, but has poorer adhesion and greater porosity. The poor adhesion characteristics of silicate watermark defects can result in the detachment of two layers which adjoin the watermark defect. For example, the poor adhesion characteristics of watermark defects 14-15 can result in STI material 13 becoming detached from substrate 11.

[0005] The relatively high porosity of a silicate watermark defect causes the watermark defect to exhibit a relatively high etch rate (with respect to silicon oxide) in the presence of HF. Thus, during subsequent HF etch steps, any exposed watermark defects will be rapidly etched, thereby creating voids where the watermark defects previously existed. These voids can result in irregularities in subsequently formed layers, thereby lowering yield and impairing device performance. For example, during an HF etch to remove pad oxide 12, silicate watermark defect 14 will be rapidly etched, thereby creating a void.

[0006] It would therefore be desirable to prevent the formation of watermarks, and thereby watermark defects, in a process that uses an HF or BOE based wet clean in the presence of a silicon oxynitride layer.

SUMMARY

[0007] Accordingly, the present invention provides a method for preventing the formation of watermark defects, particularly before the formation of shallow trench isolation structures. In one embodiment, a method for preventing the formation of watermark defects includes the steps of sequentially forming a pad oxide layer, a silicon nitride layer and a silicon oxynitride layer over a semiconductor substrate. A photoresist mask is formed over the resulting structure, with the silicon oxynitride layer being used as an anti-reflective coating during an exposure step performed during formation of the photoresist mask. An etch is performed through one or more openings in the photoresist mask, thereby forming one or more corresponding trenches in the semiconductor substrate. After the etch is completed, the photoresist mask is stripped.

[0008] After the photoresist mask has been stripped, the silicon oxynitride layer is conditioned. For example, the silicon oxynitride layer may be conditioned by a rapid thermal anneal in the presence of oxygen or nitrogen. Alternatively, the surface of the silicon oxynitride layer may be conditioned at a low temperature in the presence of oxygen. The conditioning step reduces the hydrogen content of the silicon oxynitride layer, thereby densifying this layer. This conditioning changes the properties of the silicon oxynitride layer, such that this layer becomes denser and less hydrophilic. That is, the wettability of the silicon oxynitride layer is reduced.

[0009] The silicon oxynitride layer is conditioned after the exposure of photoresist mask, such that the original anti-reflective optical properties of the silicon oxynitride layer are not modified until after these properties are no longer required.

[0010] A wet clean step is then performed to remove native oxide from the trenches. The conditioned silicon oxynitride layer advantageously prevents the formation of watermarks during this wet clean process. As a result, the formation of watermark defects is prevented during subsequent processing steps.

[0011] After the wet clean has been performed, a liner oxidation layer is thermally grown in the trenches. A shallow trench isolation (STI) layer is then deposited over the resulting structure. A chemical mechanical polishing (CMP) step can then be performed to remove the conditioned silicon oxynitride layer, a portion of the silicon nitride layer and excess STI material.

[0012] The present invention will be more fully understood in view of the following description and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Fig. 1 is a cross-sectional diagram of a conventional shallow trench isolation semiconductor structure having watermark defects.

[0014] Figs. 2-9 are cross-sectional diagrams of a semiconductor process for preventing the formation of watermark defects during shallow trench isolation in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

[0015] Figs. 2-9 are cross-sectional diagrams of a semiconductor process for preventing the formation of watermark defects in accordance with one embodiment of the present invention.

[0016] As illustrated in Fig. 2, semiconductor structure 100 includes semiconductor substrate 101, pad oxide 102, silicon nitride layer 103, silicon oxynitride layer 104 and photoresist mask 105. In the described embodiment, semiconductor substrate 101 is a lightly doped monocrystalline silicon substrate having a crystal structure of <1,0,0>. However, other semiconductor substrates can be used in other embodiments of the invention.

[0017] In the described embodiment, pad oxide 102 is a layer of silicon oxide that is thermally grown at the upper surface of substrate 101 to a thickness in the range of about 80 to 150 Angstroms. Pad oxide 102 is grown using processing techniques that are well known to those of ordinary skill in the art.

[0018] Silicon nitride (SiN) layer 103 is then deposited over pad oxide 102 to a thickness in the range of about 1300 to 1700 Angstroms. Silicon nitride layer 103 is deposited using a LPCVD process in which dichlorosilane (DCS) reacts with ammonia (NH_3) (DCS:NH_3 ratio = 1:3) at a temperature of about 800°C and a pressure of 120-200 mtorr. As described in more detail below, silicon nitride layer 103 forms a hard mask during a subsequent trench etching step.

[0019] Silicon oxynitride layer 104 is plasma-enhanced chemical vapor deposited over silicon nitride layer 103 to a thickness in the range of about 200 to 400 Angstroms. In the described embodiment, silicon oxynitride layer 104 is deposited using a process in which silane (SiH_4) reacts with nitrous oxide (N_2O) at a temperature of 350°C and a pressure of 5.5 Torr. Silicon oxynitride layer 104 forms an anti-reflective coating (ARC), which improves the quality of exposure during a subsequent photolithography step. During the initial deposition of silicon oxynitride layer 104, the SiH_4:N_2O ratio is about 1:2, such that a lower sub-layer of silicon oxynitride layer 104 comprises SiON. Subsequently, the SiH_4:N_2O ratio is changed to about 1:30 (in-

situ), such that a thin upper sub-layer of silicon oxynitride layer 104 comprises silicon oxide. As defined herein, silicon oxynitride layer 104 includes both of these sub-layers.

[0020] In addition, silicon oxynitride layer 104 has a composition of $Si_XO_YN_ZH_A$, and has a relatively large porosity. The high porosity of silicon oxynitride layer 104 causes this layer to be very hydrophilic. That is, layer 104 has a tendency to trap liquid. More specifically, silicon oxynitride layer 104 exhibits a nearly 0-degree contact angle with respect to a drop of liquid located on the surface of layer 104. This means that silicon oxynitride layer 104 exhibits almost perfect wettability.

[0021] A layer of photoresist material is deposited over silicon oxynitride layer 104. This photoresist layer is exposed through a reticle and then developed and cured, thereby forming photoresist mask 105, which includes opening 106. Opening 106 defines the location of a trench to be formed in substrate 101. Note that silicon oxynitride layer 104 prevents reflection of the light source used to expose the photoresist layer, thereby allowing opening 106 to be formed in a precise manner.

[0022] As illustrated in Fig. 3, an etch is performed through opening 106, thereby removing the exposed portion of silicon oxynitride layer 104. This etch continues through silicon nitride layer 103, through pad oxide 102, and into substrate 101, thereby forming trench 107. Trench 107 has a depth in the range of about 3000 to 5000 Angstroms. The sidewalls of trench 107 are formed at angles determined by the crystalline structure of substrate 101. In accordance with one embodiment, this etch is a high-density plasma etch performed in-situ using a $HBr/Cl_2/CF_4$ chemistry.

[0023] As illustrated in Fig. 4, photoresist mask 105 is stripped by conventional clean/ash and clean steps. In general,

the ashing step uses O_2 plus a forming gas of N_2/H_2 at a temperature of roughly 100-150°C and a low pressure.

[0024] After photoresist mask 105 has been removed, silicon oxynitride layer 104 is conditioned, thereby creating a modified silicon oxynitride layer 104A. Conditioned layer 104A exhibits improved characteristics in view of subsequently performed processing steps. Because silicon oxynitride layer 104 is conditioned after photoresist mask 105 has been patterned, the optical properties of layer 104 are not modified until after these optical properties are no longer required. Thus, the conditioning step can be performed any time after the patterning of photoresist mask 105, but before the next wet clean operation.

[0025] In the described embodiment, the conditioning step involves densifying the structure of silicon oxynitride layer 104. This conditioning step further involves reducing the hydrogen content of silicon oxynitride layer 104. In one embodiment, silicon oxynitride layer 104 is conditioned in a furnace in the presence of O_2 or N_2. In an alternate embodiment, the conditioning of silicon oxynitride layer 104 is accomplished using a rapid thermal anneal (RTA) in the presence of O_2 or N_2. In one embodiment, a RTA is performed in the presence of O_2 for 20 seconds at a temperature of 900°C. Note that O_2 is more effective than N_2 for reducing the H_2 present in silicon oxynitride layer 104. Also note that the parameters of the RTA are limited by the integration scheme for dopant diffusion.

[0026] At the end of the RTA, the conditioned silicon oxynitride layer 104A has a composition of $Si_XO_{Y+}N_ZH_{A-}$, where Y+ is greater than Y, and A- is less than A. As a result of the increased density and reduced hydrogen composition, conditioned silicon oxynitride layer 104A is substantially hydrophobic. More specifically, the contact angle of a drop of liquid located on the surface of conditioned silicon oxynitride layer 104A would be

significantly greater than 0-degrees, or on the order of about 30-50 degrees. Thus, conditioned silicon oxynitride layer 104A is significantly less wettable than original silicon oxynitride layer 104. As a result, conditioned silicon oxynitride layer 104A will have a lower etch rate in HF than original silicon oxynitride layer 104. Consequently, conditioned silicon oxynitride layer 104A is much less likely than original silicon oxynitride layer 104 to generate watermarks during an HF etch. As a result, watermark defects are virtually eliminated.

[0027] In an alternate embodiment, the surface of silicon oxynitride layer 104 is conditioned in-situ at a relatively low temperature, in the range of 300 to 400°C, using a high-density O_2-plasma treatment. This plasma treatment is performed at a pressure of around 5.5 Torr, and an O_2 flow of about 50 standard liters per minute (slpm) or higher. This low temperature surface conditioning advantageously prevents the entire silicon oxynitride layer 104 from being altered in response to a high temperature anneal. This surface conditioning prevents the formation of watermark defects during a subsequent wet clean step.

[0028] After silicon oxynitride layer 104 has been conditioned to form layer 104A, additional process steps, not relevant to the present invention, are performed on areas of substrate 101 that are not illustrated in Fig. 4. Some exemplary process steps include forming another photoresist mask, performing an angled implant to implant the sidewalls of the trench, and stripping the photoresist mask.

[0029] As illustrated in Fig. 5, a thin native oxide layer 108 is formed over the sidewalls and bottom of cavity 107 after the additional process steps have been performed. In the described embodiment, this native oxide layer 108 has a thickness in the range of about 15 to 20 Angstroms.

[0030] As illustrated in Fig. 6, oxide layer 108 is removed using a HF or BOE wet clean step. In the described embodiment, the wet clean step is performed using a 10:1 HF solution for 10-20 seconds. The wet clean step creates a substantially defect-free trench 109 having rounded edges. Note that the wet clean step undercuts pad oxide 102 to provide rounded edges at the top of trench 109. These rounded edges promote the complete filling of trench 109 with insulating material during subsequent steps. Advantageously, conditioned silicon oxynitride layer 104A does not react with the HF solution used during the wet etch to create watermarks. This is probably because silicon oxynitride layer 104A is relatively dense, and does not easily trap the HF solution. As a result, no watermarks are located on conditioned silicon oxynitride layer 104A or in trench 109 at the end of the wet clean step.

[0031] As illustrated in Fig. 7, liner oxidation layer 110 is thermally grown at the sidewalls and bottom of trench 109. In the described embodiment, liner oxidation layer 110 is silicon oxide grown to a thickness in the range of 300 to 500 Angstroms in a dry O_2 atmosphere at a temperature in the range of about 1000 to 1150°C. In a particular embodiment, liner oxidation layer 110 is grown to a thickness of about 400 Angstroms. Because there are no watermarks located in trench 109, no watermark defects are formed adjacent to liner oxidation layer 110.

[0032] As illustrated in Fig. 8, a shallow trench insulating (STI) layer 111 is deposited over the resulting structure. In the described embodiment, STI layer 111 is a layer of silicon oxide having a thickness of about 8000 Angstroms. STI layer 111 is deposited using a conventional STI filling process, such as a high-density plasma (HDP) or sub-atmosphere CVD (SACVD) process. If a HDP process is used, an $O_2/SiH_4/Ar$ chemistry is used in the presence of a very low pressure.

[0033] As illustrated in Fig. 9, a chemical-mechanical polishing (CMP) step is then performed to remove the upper portion of STI layer 111, conditioned silicon oxynitride layer 104A and a portion of silicon nitride layer 103. The CMP step is targeted to stop with about 1000 Angstroms of silicon nitride layer 103 remaining.

[0034] The portion of STI layer 111 located in trench 109, hereinafter referred to as shallow trench isolation (STI) structure 111A, is not removed by the CMP step. Because no watermarks were present in trench 109 (i.e., on liner oxidation 110) when STI layer 111 was deposited, no watermark defects are formed between the liner oxidation 110 and STI structure 111A. As a result, there is a relatively strong adhesion between STI structure 111A and liner oxidation 110, thereby preventing STI structure 111A from tearing off during the CMP step.

[0035] Moreover, because there are no watermark defects exposed adjacent to STI structure 111A at the upper surface of the resulting structure, subsequent HF-based wet cleaning steps will not create voids at the interfaces of STI structure 111A, liner oxidation layer 110 and trench 109.

[0036] Although the invention has been described in connection with several embodiments, it is understood that this invention is not limited to the embodiments disclosed, but is capable of various modifications, which would be apparent to a person skilled in the art. For example, although the present invention has been described in connection with the fabrication of an STI structure, the present invention is applicable to other processes where HF or BOE based wet cleaning is performed in the presence of silicon oxynitride. Moreover, although the formation of one STI region has been described, it is understood that many STI regions can be formed at the same time. Thus, the invention is limited only by the following claims.